## AMENDMENT TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Please cancel claims 44 - 105.

**Listing of Claims:**

1. (Amended) A circuit for use in a digital display unit **[of a computer system, and circuit]** for generating a plurality of pixel data elements from an analog image data received by said digital display unit, said digital display unit further receiving a time reference signal associated with said analog image data, said time reference signal having a high frequency, said circuit comprising:

an analog-to-digital converter (ADC) for receiving said analog image data, said ADC sampling said analog image data using a sampling clock to generate a plurality of pixel data elements corresponding to said plurality of pixels, wherein said sampling clock has a sampling frequency equal to said high frequency;

a clock generator circuit comprising a phase-locked loop (PLL) circuit for generating said sampling clock, wherein said sampling clock is synchronized with said time reference signal with a jitter of less than a few nano-seconds, said PLL comprising:

a discrete time oscillator (DTO) for receiving a digital input and generating a signal representative of said sampling clock with a frequency determined by said digital input; and

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said DTO to generate said signal synchronized with said time reference signal, said digital circuit comprising:

a frequency correction logic for adjusting the phase of said sampling clock according to the long-term drifts in the frequency of said time reference signal; and

a phase correction logic for adjusting the phase of said sampling clock according to the phase difference in said feedback signal and said time reference signal,

wherein said frequency correction logic and said phase correction logic are implemented as two separate control loops,

wherein a panel interface included in said digital display unit can generate display signals for a display screen based on said plurality of pixel data elements.

2. (Original) The circuit of claim 1, wherein said clock generator circuit further comprises an analog filter to eliminate any undesirable frequencies from said signal representative of said sampling clock to generate said sampling clock.

3. (Original) The circuit of claim 1, further comprising a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal.

4. (Original) The circuit of claim 3, further comprising a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of said difference of phase.

5. (Original) The circuit of claim 1, wherein said analog image data and said time reference signal are received on two separate signal paths.

6. (Original) The circuit of claim 5, wherein said reference clock comprises a binary signal.

7. (Original) The circuit of claim 1, wherein said digital circuit distributes phase error between said feedback signal and said reference signal during a comparison cycle by changing the phase of individual clock pulses in said sampling clock.

8. (Original) The circuit of claim 1, wherein said frequency correction logic generates a multi-bit number, wherein said multi-bit number is representative of the amount of phase advance of said sampling clock generated by said DTO during a DTO clock period, and wherein said multi-bit representation enables said PLL to reach said sampling frequency within a short duration.

9. (Original) The circuit of claim 1, wherein said frequency correction logic comprises:

a first multiplexor accepting as input Pnom and Fdp values, wherein Pnom represents an expected frequency of said sampling clock and Fdp represents the correction due to the long-term frequency drifts;

a flip-flop for storing a value representative of the phase correction corresponding to the frequency correction logic;

an adder for adding or subtracting the output of said first multiplexor from the value stored in said flip-flop, wherein the output of said adder is stored in said flip-flop; and

a frequency correction control coupled to said flip-flop and said adder, wherein said frequency correction control causes said flip-flop to be set to Pnom at the beginning of a phase acquisition phase, and wherein said frequency correction control causes said adder to add or subtract Fdp depending on whether the sampling clock is early or late in comparison to said time reference.

10. (Original) The circuit of claim 1, further comprising:

a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal, wherein said phase and frequency detector asserts an EARLY signal a number of clock pulses proportionate to the difference of phase by which said feedback signal is earlier than said time reference signal and a or a LATE signal a number of pulses proportionate to the difference of phase by which said feedback signal is later than said time reference signal; and

a charge/discharge control logic implemented using digital components, said charge/discharge control logic including a phase integrator, said charge/discharge control logic charging said phase integrator according to the number of pulses said EARLY signal or said LATE signal is asserted, said charge/discharge logic discharging over a longer period of time than the charging period so as to spread the difference in phase over a comparison cycle, wherein the phase of said sampling clock is corrected during the discharging period.

11. (Original) The circuit of claim 10, further comprising a sign and zero crossing detector for correcting any over-correction performed by said charge/discharge logic during said discharging period.

12. (New) A circuit for use with a digital display unit for generating a plurality of digital image data elements from analog image data received by said digital display unit, wherein said digital display unit further receives a time reference signal having a time reference signal frequency associated with said analog image data, said circuit comprising:

an analog-to-digital converter (ADC) for sampling said analog image data using a sampling clock to generate said plurality of digital image data elements;

a clock generator circuit for generating said sampling clock that is synchronized with said time reference signal and that receives a digital input and generates a signal representative of said sampling clock with a frequency determined by said digital input; and

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said clock generator circuit to generate said signal synchronized with said time reference signal.

13. (New) The circuit of claim 12, wherein said clock generator circuit further comprises:

an analog filter to eliminate any undesirable frequencies from said signal representative of said sampling clock to generate said sampling clock; and

a phase-locked loop (PLL) circuit that includes a discrete time oscillator (DTO).

14. (New) The circuit of claim 12, further comprising a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal.

15. (New) The circuit of claim 14, further comprising a charge/discharge control logic for determining the amount of phase correction to be made based on the determination of said difference of phase.

16. (New) The circuit of claim 12, wherein said analog image data and said time reference signal are received on two separate signal paths.

17. (New) The circuit of claim 16, wherein said reference clock comprises a binary signal.

18. (New) The circuit as recited in claim 12, wherein said sampling clock has a sampling frequency equal to said time reference signal frequency.

19. (New) The circuit as recited in claim 12, further comprising:

a frequency correction logic for adjusting the phase of said sampling clock according to the long-term drifts in said time reference signal frequency; and

a phase correction logic for adjusting the phase of said sampling clock according to the phase difference in said feedback signal and said time reference signal,

wherein said frequency correction logic and said phase correction logic are implemented as two separate control loops.

20. (New) The circuit as recited in claim 12, wherein said digital display comprises:

a display screen; and

a panel interface arranged to generate display signals for the display screen based on said plurality of digital image data elements.

21. (New) The circuit of claim 19, wherein said digital circuit distributes phase error between said feedback signal and said reference signal during a comparison cycle by changing the phase of individual clock pulses in said sampling clock.

22. (New) The circuit of claim 19, wherein said frequency correction logic generates a multi-bit number, wherein said multi-bit number is representative of the amount of phase advance of said sampling clock generated by said DTO during a DTO clock period, and wherein said multi-bit representation enables said PLL to reach said sampling frequency within a short duration.

23. (New) The circuit of claim 19, wherein said frequency correction logic comprises:

a first multiplexor accepting as input Pnom and Fdp values, wherein Pnom represents an expected frequency of said sampling clock and Fdp represents the correction due to the long-term frequency drifts;

a flip-flop for storing a value representative of the phase correction corresponding to the frequency correction logic;

an adder for adding or subtracting the output of said first multiplexor from the value stored in said flip-flop, wherein the output of said adder is stored in said flip-flop; and

a frequency correction control coupled to said flip-flop and said adder, wherein said frequency correction control causes said flip-flop to be set to Pnom at the beginning of a phase acquisition phase, and wherein said frequency correction control causes said adder to add or subtract Fdp depending on whether the sampling clock is early or late in comparison to said time reference.

24. (New) The circuit of claim 12, further comprising:

a phase and frequency detector for determining the difference of phase between said feedback signal and said time reference signal, wherein said phase and frequency detector asserts an EARLY signal a number of clock pulses proportionate to the difference of phase by which said feedback signal is earlier than said time reference signal and a or a LATE signal a number of pulses proportionate to the difference of phase by which said feedback signal is later than said time reference signal; and

a charge/discharge control logic implemented using digital components, said charge/discharge control logic including a phase integrator, said charge/discharge control logic charging said phase integrator according to the number of pulses said EARLY signal or said

LATE signal is asserted, said charge/discharge logic discharging over a longer period of time than the charging period so as to spread the difference in phase over a comparison cycle, wherein the phase of said sampling clock is corrected during the discharging period.

25. (New). The circuit of claim 24, further comprising a sign and zero crossing detector for correcting any over-correction performed by said charge/discharge logic during said discharging period.

26. (New) A method of providing a destination image frame formed of a number of destination image elements, comprising:

receiving source image elements in accordance with a source frame rate;

scaling said source image elements independently in both vertical and horizontal directions to form said destination image elements; and

providing said destination image elements in accordance with a destination frame rate, wherein said source frame rate is substantially equal to said destination frame rate.

27. (New) A method of claim 26, wherein a source image includes a plurality of source image frames, and wherein a destination image corresponding to said source image is generated by generating a destination image frame corresponding to each of said source image frames.

28. (New) A method as recited in claim 26, wherein when said scaling is upscaling, said scaling further comprises:

replicating a plurality of said source image elements to obtain replicated source image elements.

29. (New) A method as recited in claim 28, said scaling further comprising:

interpolating selected ones of said source image elements and said replicated source image elements to generate said destination image elements.

30. (New) A method as recited in claim 29, wherein said source image frame includes a plurality of source scan lines each of which includes a number of said source image elements, and wherein the destination image frame includes a plurality of destination scan lines each of which includes a number of said destination image elements.

31. (New) A method as recited in claim 30, further comprising:

using at least a present scan line and a previous scan line for said interpolation, wherein said present scan line and said previous scan line are included in said plurality of source scan lines.

32. (New) A method of claim 31, wherein at least one of said source scan lines is used one or more times as a present scan line.

33. (New) A method as recited in claim 26, wherein said source image frame has an associated source image frame aspect ratio and wherein said destination image frame has an associated destination image frame aspect ratio, wherein said scaled destination image frame aspect ratio is different from said source image frame aspect ratio.

34. (New) A method as recited in claim 26, wherein said source frame rate is based upon a first clock signal and wherein said destination frame rate is based upon a second clock signal.

35. (New) A method as recited in claim 34, further comprising:

storing said source image elements being received into a line buffer in accordance with said second clock signal; and

thereafter, outputting said destination image elements in accordance with said second clock signal.

36. (New) A method of claim 35, wherein said second clock signal is locked to said first clock signal in a proportion.

37. (New) A method of claim 36, wherein said proportion is equal to a ratio of a total number of source image elements to a total number of destination image elements.

38. (New) A digital display unit having a display screen for displaying a destination image frame formed of a number of destination image elements, comprising:

a display unit interface for displaying the destination image frame at a display rate based upon a display clock signal;

a converter circuit for generating a plurality of digital source image elements from an analog source image received by said digital display unit based upon a sampling clock signal wherein the analog source image has a associated time reference signal and time reference signal frequency;

a scaler unit coupled to the converter circuit arranged to

receive said digital source image elements at a line buffer in accordance with a destination clock signal,

scale said source image elements independently in both vertical and horizontal directions to form said destination image elements, and

provide said destination image elements in accordance with the destination clock signal to the display unit interface wherein a source frame rate and a destination frame rate are related so as to not overflow the line buffer over a period of time; and

a clock circuit arranged to produce the display clock signal, the sampling clock signal, the first clock signal and the second clock signal, wherein the sampling clock is synchronized with the time reference signal.

39. (New) A digital display unit as recited in claim 38, wherein the clock circuit receives a digital input and generates a signal representative of said sampling clock with a frequency determined by said digital input.

40. (New) A digital display unit as recited in claim 39, further comprising:

a digital circuit for receiving said time reference signal and a feedback signal, wherein said feedback signal is generated by dividing said sampling clock, said digital circuit generating said digital input according to the difference of the phases of said time reference signal and said feedback signal, said digital input causing said clock circuit to generate said sampling clock signal synchronized with said time reference signal.

41. (New) A method of displaying an analog source image by a digital display unit having a display screen as a destination image frame formed of a number of destination image elements wherein the analog source image has a associated time reference signal and time reference signal frequency, comprising:

synchronizing a sampling clock signal to the time reference signal;

generating a plurality of digital source image elements from said analog source image based upon said sampling clock signal;

scaling said digital source image elements by a scaler unit by

receiving said digital source image elements at a source frame ratel, and

scaling said source image elements independently in both vertical and horizontal directions to form said destination image elements; and

providing said destination image elements at a destination frame rate in accordance to the display unit interface at a rate that does not overflow the line buffer on average; and

displaying the destination image elements by the digital display.

42. (New) A method as recited in claim 41, further comprising:

receiving a digital input that causes said clock circuit to generate said signal synchronized with said time reference signal; and

generating a signal representative of said sampling clock with a frequency determined by said digital input.

43. (New) A method as recited in claim 42, comprising:

generating a feedback signal by dividing said sampling clock; and

receiving said time reference signal and a feedback signal, wherein the digital input is based upon the difference of the phases of said time reference signal and said feedback signal.

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106. (New) A circuit for use in a digital display unit for generating a plurality of image pixel data elements for display on a display screen, comprising:

a source interface arranged to receive source image pixels from a source image, said source interface includes an analog-to-digital converter (ADC) for sampling said source image pixels using a sampling clock to generate a plurality of pixel data elements;

a clock generator circuit for generating said sampling clock; and

an upscaler for upscaling said source image to a destination image having more pixels than does the source image, comprising:

a line buffer arranged to receive and store pixel data elements from the source interface; and

a display interface arranged to receive pixel data elements from the line buffer and provide the plurality of image pixel elements for display without using a frame buffer.

107. (New) A circuit as recited in claim 106, wherein the display interface further comprises:

an interpolator coupled to the line buffer and arranged to provide the plurality of destination image pixel elements using pixel data elements stored in and read from said line buffer.

108. (New) A circuit as recited in claim 107, wherein said interpolator comprises:

a vertical interpolator unit arranged to vertically interpolate pixel data elements received from said line buffer; and

a horizontal interpolator unit coupled to the vertical interpolator unit arranged horizontally interpoloate selected ones of the vertically interpolated pixel data elements.

109. (New) A circuit as recited in claim 108, wherein the interpolator further comprises:

a first interpolation line buffer coupled to the vertical interpolator and the line buffer for storing previous vertically interpolated pixel data elements; and

a second interpolation line buffer for storing current vertically interpolated pixel data elements that are used by the horizontal interpolater unit to carry out the horizontal interpolation.

110. (New) A circuit as recited in claim 106, wherein the line buffer is a single port memory type line buffer that includes a single port SDRAM.

111. (New) A circuit as recited in claim 106, wherein the line buffer is a dual ported memory type line buffer.

112. (New) A circuit as recited in claim 110 wherein when the line buffer is the single port SDRAM, then the line buffer includes a first memory bank and a second memory bank.

113. (New) A circuit as recited in claim 112, wherein when pixel data elements corresponding to a source image scan line is received in the first bank, then pixel data elements corresponding to another source image scan line can be concurrently read from the second memory bank as many times as required.

114. (New) A circuit as recited in claim 111, wherein when said line buffer is the dual-ported memory, pixel data elements are read from a port that is different from a port that receives the pixel data elements.

115. (New) A method for generating a plurality of image pixel data elements for display on a display screen, comprising:

receiving source image pixels from a source image;

generating a plurality of pixel data elements by sampling said source image pixels;

receiving and storing pixel data elements at a line buffer;

receiving pixel data elements from the line buffer;

providing the plurality of image pixel elements for display without using a frame buffer; and

displaying a destination image having more pixels than does the source image using the provided plurality of image pixel elements.